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Amdt. dated March 25, 2004
Reply to Office action of January 20, 2004

<u>Amendments to the Specification:</u>

Please replace the paragraph beginning at page 1, line 8, with the following rewritten paragraph:

This application relates to the following commonly assigned co-pending applications entitled:

"Apparatus And Method For Interfacing A High Speed Scan-Path With Slow-Speed Test Equipment," Serial No. 09/653,642————, filed August 31, 2000, Attorney Docket No. 1662-23700; "Rotary Rule And Coherence Dependence Priority Rule," Serial No. ————, filed August 31, 2000, Attorney Docket No. 1662-27300; "Speculative Scalable Directory Based Cache Coherence Protocol," Serial No. 09/652,703————, filed August 31, 2000, Attorney Docket No. 1662-27400; "Scalable Efficient I/O Port Protocol," Serial No. 09/652,391————, filed August 31, 2000, Attorney Docket No. 1662-27500; "Efficient Translation <u>Lookaside</u> Buffer Miss Processing <u>In Computer For</u> Applications Using Large Pages In Systems With A Large Range Of Page Sizes By Eliminating Page Table Level," Serial No. 09/652,552————, filed August 31, 2000, Attorney Docket No. 1662-27600; "Fault Containment And Error Recovery Techniques In A Scalable Multiprocessor," Serial No. 09/651,949————, filed August 31, 2000, Attorney Docket No. 1662-27700; "Speculative Directory Writes In A Directory Based Cache Coherent Nonuniform Memory Access Protocol," Serial No. 09/652,834————, filed August 31, 2000, Attorney Docket No. 1662-27800; "Special Encoding Of Known Bad Data," Serial No. 09/652,314————, filed August 31, 2000, Attorney Docket No. 1662-27900; "Broadcast Invalidate Scheme," Serial No. 09/652,165————, filed August 31, 2000, Attorney Docket No. 1662-28000; "<u>Mechanism To Track All Open Pages In A DRAM Memory System," Serial No. 09/652,704, filed August 31, 2000;</u> "Programmable DRAM Address Mapping Mechanism," Serial No. 09/653,093————, filed August 31, 2000, Attorney Docket No. 1662-28200; "<u>Computer Architecture And System For Efficient Management Of Bi-Directional Bus</u>Mechanism To Enforce Memory Read/Write Fairness, Avoid Tristate Bus Conflicts, And Maximize Memory Bandwidth," Serial No. 09/652,323————.

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filed August 31, 2000, Attorney Docket No. 1662-29200; "An Efficient Address Interleaving With Simultaneous Multiple Locality Options," Serial No. 09/652,452————————, filed August 31, 2000, Attorney Docket No. 1662-29300; "A High Performance Way Allocation Strategy For A Multi-Way Associative Cache System," Serial No. 09/653,092——————————, filed August 31, 2000, Attorney Docket No. 1662-29400; "Method And System For Absorbing Defects In High Performance Microprocessor With A Large N-Way Set Associative Cache," Serial No. 09/651,948—————————, filed August 31, 2000, Attorney Docket No. 1662-29500; "A Method For Reducing Directory Writes And Latency In A High Performance, Directory-Based, Coherency Protocol," Serial No. 09/652,324—————————, filed August 31, 2000, Attorney Docket No. 1662-29600; "Mechanism To Reorder Memory Read And Write Transactions For Reduced Latency And Increased Bandwidth," Serial No. 09/653,094————————, filed August 31, 2000, Attorney Docket No. 1662-30800; "System For Minimizing Memory Bank Conflicts In A Computer SystemLook-Ahead Mechanism To Minimize And Manage Bank Conflicts In A Computer Memory System," Serial No. 09/652,325—————————, filed August 31, 2000, Attorney Docket No. 1662-30900; "Computer Resource Management And Allocation System," Serial No. 09/651,945—————————, filed August 31, 2000, Attorney Docket No. 1662-31000; "Input Data Recovery Scheme," Serial No. 09/653,643—————————, filed August 31, 2000, Attorney Docket No. 1662-31100; "Fast Lane Prefetching," Serial No. 09/652,451—————————, filed August 31, 2000, Attorney Docket No. 1662-31200; "Mechanism For Synchronizing Multiple Skewed Source-Synchronous Data Channels With Automatic Initialization Feature," Serial No. 09/652,480—————————, filed August 31, 2000, Attorney Docket No. 1662-31300; "Mechanism To Control The Allocation Of An N-Source Shared Buffer," Serial No. 09/651,924—————————, filed August 31, 2000, Attorney Docket No. 1662-31400; and "Chaining Directory Reads And Writes To Reduce DRAM Bandwidth In A Directory Based CC-NUMA Protocol," Serial No. 09/652,315—————————, filed August 31, 2000, Attorney Docket No. 1662-31500, all of which are incorporated by reference herein.